Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A full depletion SOI-MOS transistor comprising:

a substrate having a main surface;

a buried oxide layer ~~formed~~ on the main surface of the substrate;

a thin silicon layer on the buried oxide layer, the thin silicon layer including a channel region and an impurity ~~diffused~~ activated source/drain region;

an isolation layer ~~formed~~ on the buried oxide layer, the isolation layer adjacent the thin silicon layer;

a gate insulation layer ~~formed~~ on the channel region of the thin silicon layer;

a gate electrode ~~formed~~ on the gate insulation layer; and

a deposited polysilicon layer on the impurity ~~diffused~~ activated source/drain region of the thin silicon layer and extending on an uppermost surface of the isolation layer, wherein the impurity ~~diffused~~ activated source/drain region and the deposited polysilicon layer together constitute a source/drain of the full depletion SOI-MOS transistor.

Claim 2 (Currently Amended): A full depletion SOI-MOS transistor according to claim 1, further comprising a sidewall ~~formed~~ on the gate insulation layer, adjacent the gate electrode.

Claim 3 (Canceled)

Claim 4 (Previously Presented): A full depletion SOI-MOS transistor according to claim 2, wherein the deposited polysilicon layer extends on the sidewall.

Claim 5 (Previously Presented): A full depletion SOI-MOS transistor according to claim 1, wherein a thickness of the thin silicon layer is about 20 to 80 percent of a total thickness of the thin silicon layer and the deposited polysilicon layer.

Claim 6 (Previously Presented): A full depletion SOI-MOS transistor according to claim 1, wherein a thickness of the thin silicon layer is less than about 35 nm.

Claims 7-12 (Canceled)

Claim 13 (Currently Amended): A full depletion SOI-MOS transistor comprising:

a substrate having a main surface;

a BOX layer ~~formed~~ on the main surface of the substrate;

an SOI layer on the BOX layer, the SOI layer including a channel region and an impurity ~~diffused~~ activated source/drain region;

an isolation layer ~~formed~~ on the BOX layer, the isolation layer adjacent the SOI layer;

a gate insulation layer ~~formed~~ on the channel region of the SOI layer;

a gate electrode ~~formed~~ on the gate insulation layer; and

a deposited high mobility conductive layer on the impurity ~~diffused~~ activated source/drain region of the thin silicon layer and extending on an uppermost surface of the isolation layer, wherein the deposited high mobility conductive layer contains polysilicon and wherein the impurity ~~diffused~~ activated source/drain region and the deposited high mobility conductive layer together constitute a source/drain of the full depletion SOI-MOS transistor.

Claim 14 (Currently Amended): A full depletion SOI-MOS transistor according to claim 13, further comprising a sidewall ~~formed~~ on the gate insulation layer, adjacent the gate electrode.

Claim 15 (Canceled)

Claim 16 (Previously Presented): A full depletion SOI-MOS transistor according to claim 14, wherein the deposited high mobility conductive layer extends on the sidewall.

Claim 17 (Previously Presented): A full depletion SOI-MOS transistor according to claim 13, wherein a thickness of the SOI layer is about 20 to 80 percent of a total thickness of the SOI layer and the deposited high mobility conductive layer.

Claim 18 (Previously Presented): A full depletion SOI-MOS transistor according to claim 13, wherein a thickness of the SOI layer is less than about 35 nm.

Claim 19 (Previously Presented): A full depletion SOI-MOS transistor according to claim 13, wherein the deposited high mobility conductive layer contains silicide.

Claim 20 (Currently Amended): A full depletion SOI-MOS transistor according to claim 19, wherein the deposited high mobility conductive layer is ~~formed~~ on the gate electrode.